APPENDIX A

Marked-Up Version of Amended Paragraphs

At paragraph 7 on pages 3-4:

Plug-and-Play ™ resource allocation programs, as required by PCI bridge specifications, typically expect the address space allocated to a particular PCI bus to include the address space allocated to any PCI bus behind that particular PCI bus. Accordingly, full compliance with PCI protocol increases the difficulty of locating PCI devices on the host processor side of a host-to-PCI bridge, where the PCI devices - possibly for compatibility reasons - require an address space that may be a subset of the address space allocated to a physical PCI bus.

BRIEF DESCRIPTION OF DRAWINGS

Figs. [1a] 1A, [1b] 1B show a system configuration in accordance with the present invention.

Fig. 2 shows a more detailed system configuration.

Fig. 3 shows a system with a primary virtual bridge.

Fig. 4 shows a system with a secondary virtual bridge and a primary virtual bridge.

Fig. 5, [5a] 6A, [6b] 6B show flow charts of method embodiments.

At paragraph 9 on page 5:

Figs. [1a] 1A, [1b] 1B, 2, 3 and 4 show block diagrams of systems 100, 200, 300 and 400 for explaining various embodiments of the present invention. Processor 130 may represent any one processor coupled to host bus 120. Alternatively processor 130 may represent two or more processors coupled to host bus 120.

At paragraph 19, page 9:

Fig. [1a] 1A shows host bus device 110 coupled to host bus through interface 112, which is distinct from the host bus interface to processor 130. Fig. [1b] 1B shows an alternate configuration consistent with the methods of the present invention, where processor 130 and host bus device 110 are coupled to host bus 120 through an internal bus 113 and a shared host bus interface 112. The system of Fig. [1b] 1B can result from integrating host bus device 110 and processor 130 into a single circuit package.

At paragraph 39, page 17:

Fig. [6a] 6A and [6b] 6B show flow diagrams for explaining a method 600 executed by monitor circuit 114 of system 400, which is shown in Fig. 4. Start (step 610) and capturing (step 620) may be the same as described for steps 510 and 520, respectively. Assessing (step 540) and snooping (step 560) are accomplished with steps 641, 642, 662 and 664. Likewise assessing step 550 and intercepting step 580 are accomplished with steps 643, 644, 645, 682, 684, and 686. Assessing steps 641-645 may

take place substantially in parallel during the address phase of a host bus cycle, and if snooping step 662, 664 or intercepting step 682, 684, 686 is executed, then the snooping or intercepting step may take place during the data phase of a host bus cycle. Snooped cycles may be completed (e.g. terminated) by a device other than host bus device 410 and intercepted cycles may be completed by the host bus device 410.